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Revision History

Rev.	Date	Designer	Comments
A	18 Apr. 05	G Rouse	Initial release.
B	30 Aug. 05	G Rouse	Changed U3 to ST LD29080. Changed U9-VIN to 3V3. Removed unnecessary jumpers. Renamed jumpers. Added 10K pullup to *ATTN. Rationalized resistors into resistor packs. Renamed MCF5208 signal names for consistency with MCF5208RM.pdf.

M5208EVB Evaluation Board

TITLE: M5208EVB_Rev_B

Document Number:

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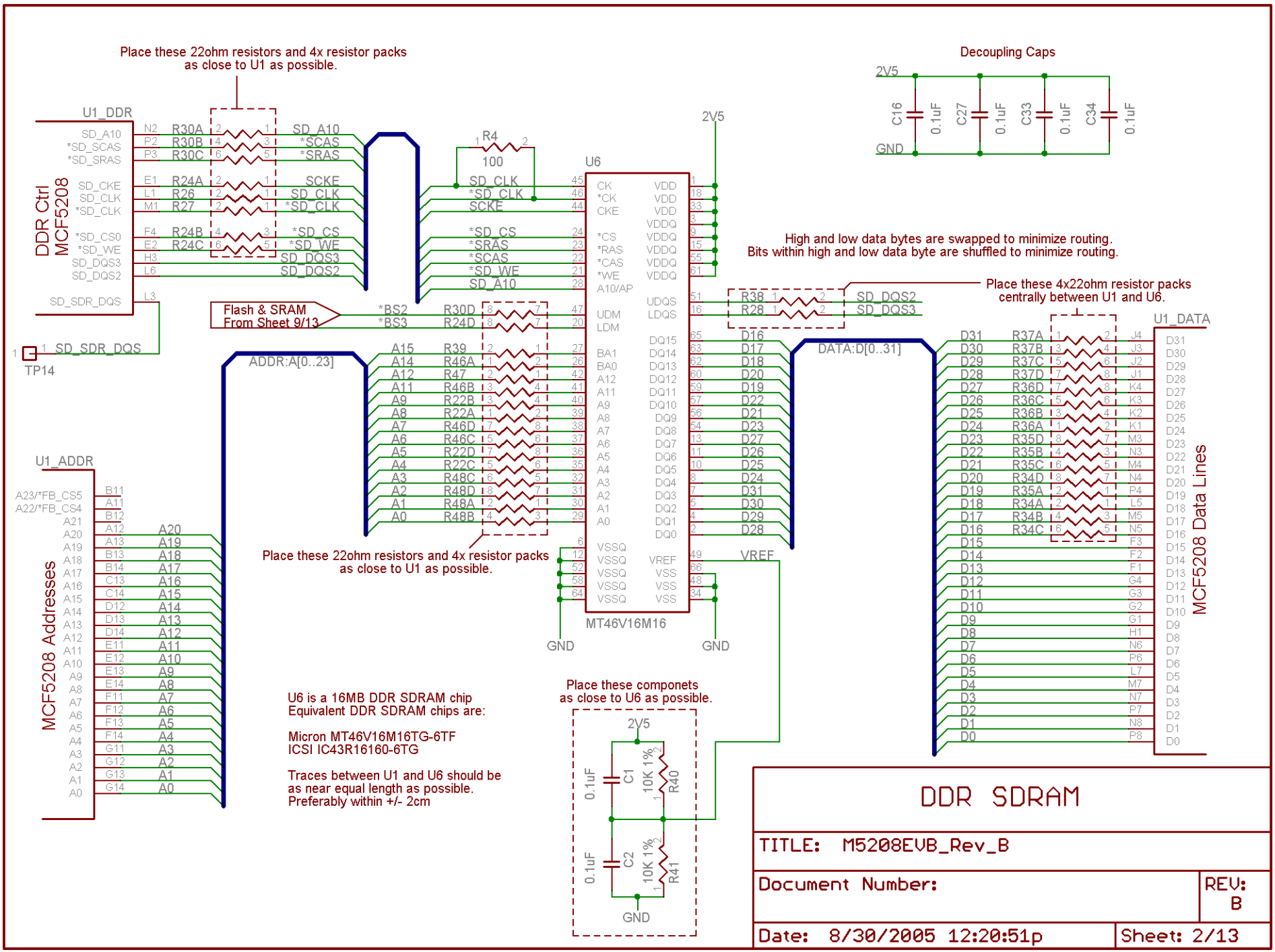
Place these 22ohm resistors and 4x resistor packs as close to U1 as possible.
U1_DDR
DDR Ctrl MCF5208
SD_A10
*SD_SCAS
*SD_SRAS
SD_CKE
SD_CLK
*SD_CLK
*SD_CS0
*SD_WE
SD_DQS3
SD_DQS2
SD_SDR_DQS
R30A
R30B
R30C
R24A
R26
R27
R24B
R24C
SCKE
*SD_CS
*SD_WE
SD_DQS3
SD_DQS2
R4
100
U6
2V5
Flash & SRAM From Sheet 9/13
*BS2
*BS3
R30D
R24D
TP14
ADDR:A[0..23]
A15
A14
A12
A11
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
R39
R46A
R47
R46B
R22B
R22A
R46D
R46C
R22D
R22C
R48C
R48D
R48A
R48B
Place these 22ohm resistors and 4x resistor packs as close to U1 as possible.
U1_ADDR
MCF5208 Addresses
A23/*FB_CS5
A22/*FB_CS4
MT46V16M16
GND
VREF
U6 is a 16MB DDR SDRAM chip
Equivalent DDR SDRAM chips are:
Micron MT46V16M16TG-6TF
ICSI IC43R16160-6TG
Traces between U1 and U6 should be as near equal length as possible.
Preferably within +/- 2cm
Place these componets as close to U6 as possible.
0.1uF
C1
10K 1%
R40
C2
R41
Decoupling Caps
C16
C27
C33
C34
High and low data bytes are swapped to minimize routing.
Bits within high and low data byte are shuffled to minimize routing.
Place these 4x22ohm resistor packs centrally between U1 and U6.
R38
R28
SD_DQS2
SD_DQS3
DATA:D[0..31]
U1_DATA
MCF5208 Data Lines
R37A
R37B
R37C
R37D
R36D
R36C
R36B
R36A
R35D
R35B
R35C
R34D
R35A
R34A
R34B
R34C
DDR SDRAM
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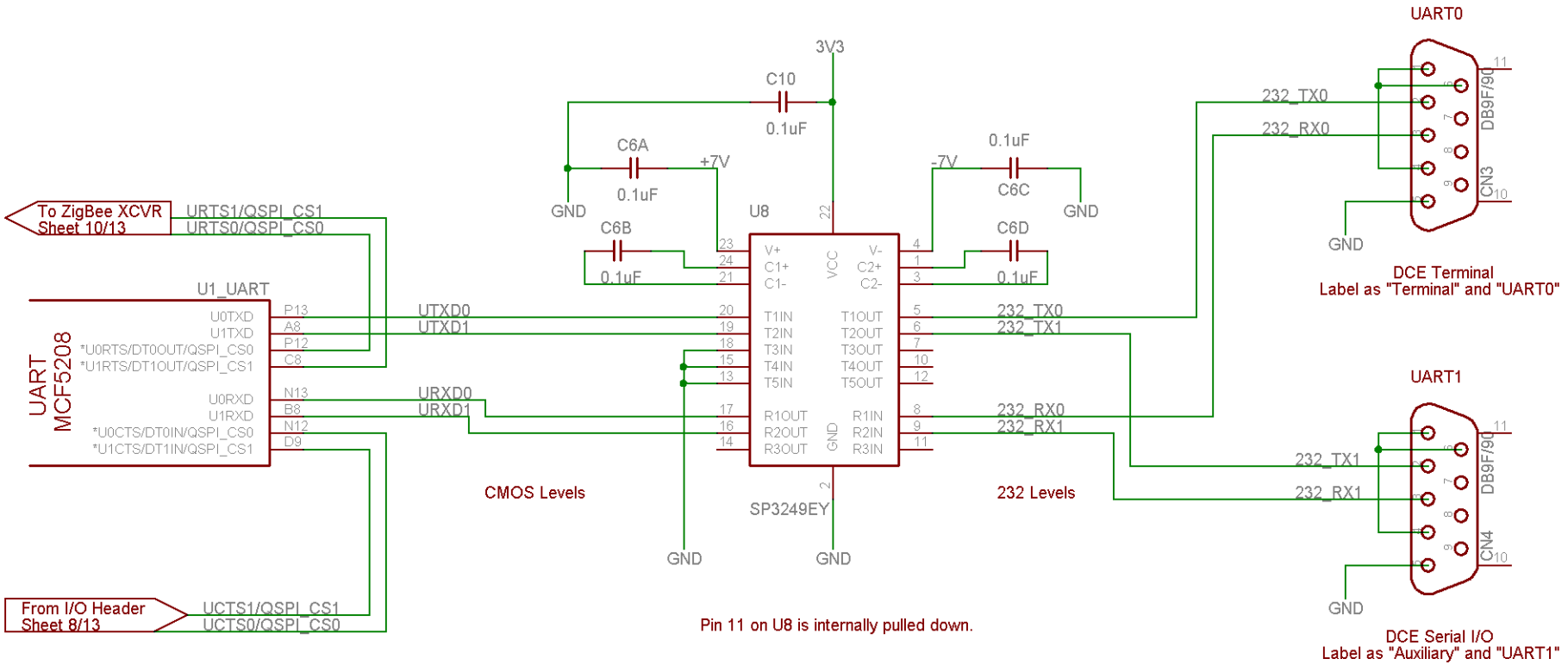

Serial Communications

TITLE: M5208EVB_Rev_B	
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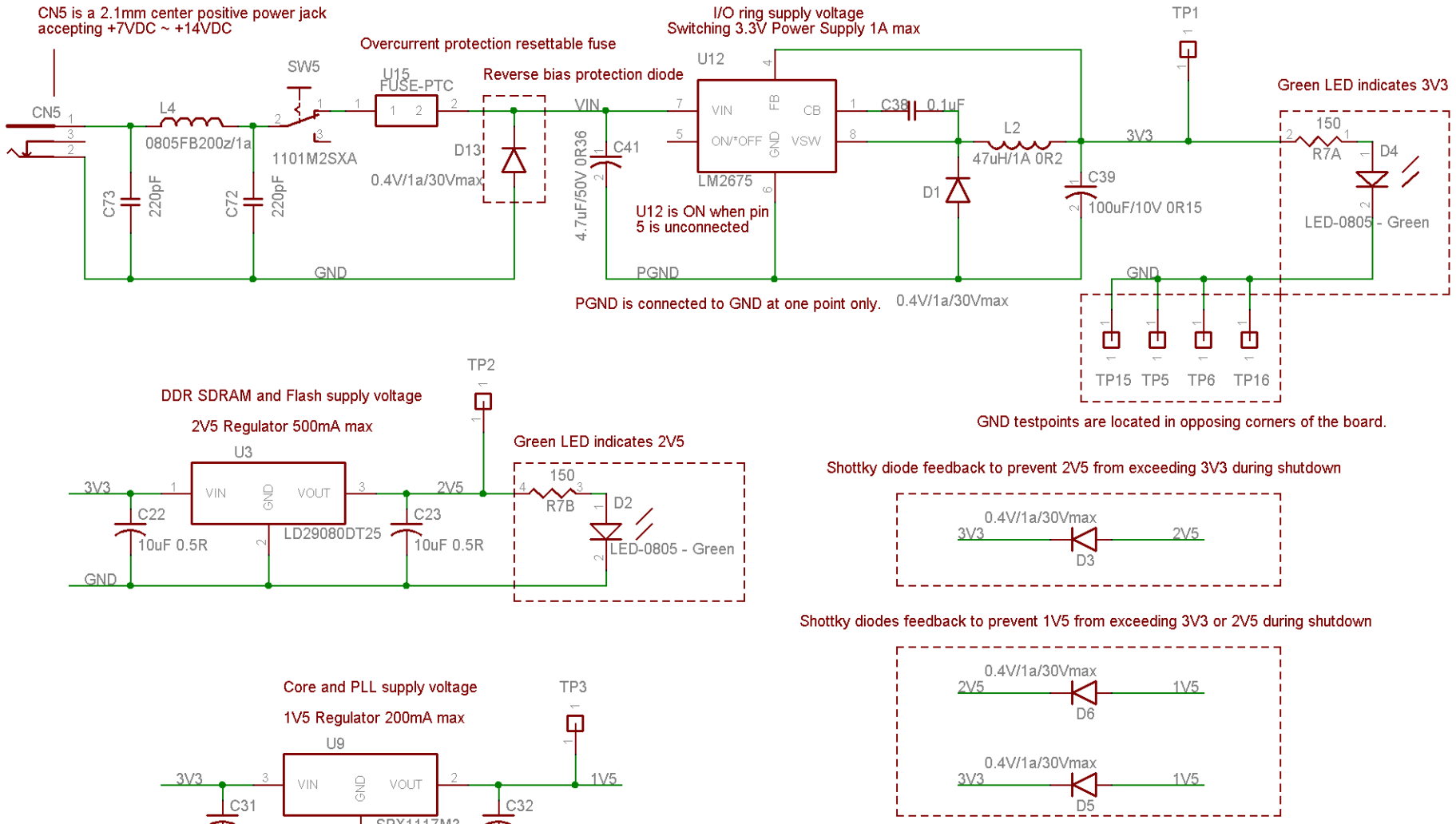

Power Supply

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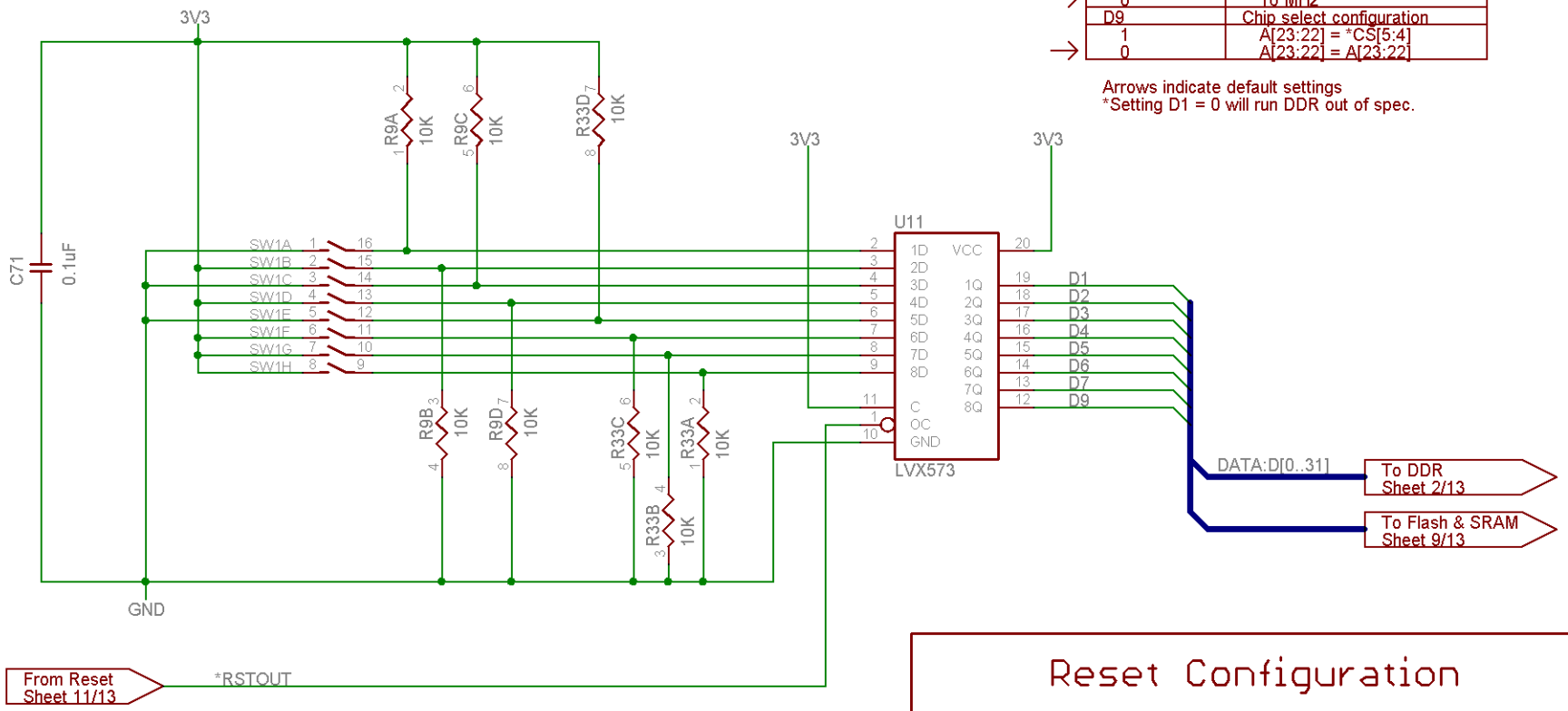
Reset Configuration

→	D1	PLL Mode
	1	166.67/83.33 MHz operation
	0	88/44 MHz operation *
→	D2	Oscillator Mode
	1	Oscillator bypass mode
	0	Crystal oscillator mode
→	D[4:3]	Boot port size
	00, 11	32-bit port
	01	16-bit port
	10	8-bit port
→	D5	Output pad drive strength
	1	High drive strength
	0	Low drive strength
→	D6	Limp mode
	1	Limp mode
	0	Normal PLL mode
→	D7	Clock Frequency Input
	1	16.67 MHz
	0	16 MHz
→	D9	Chip select configuration
	1	A[23:22] = *CS[5:4]
	0	A[23:22] = A[23:22]

Arrows indicate default settings
*Setting D1 = 0 will run DDR out of spec.



Reset Configuration

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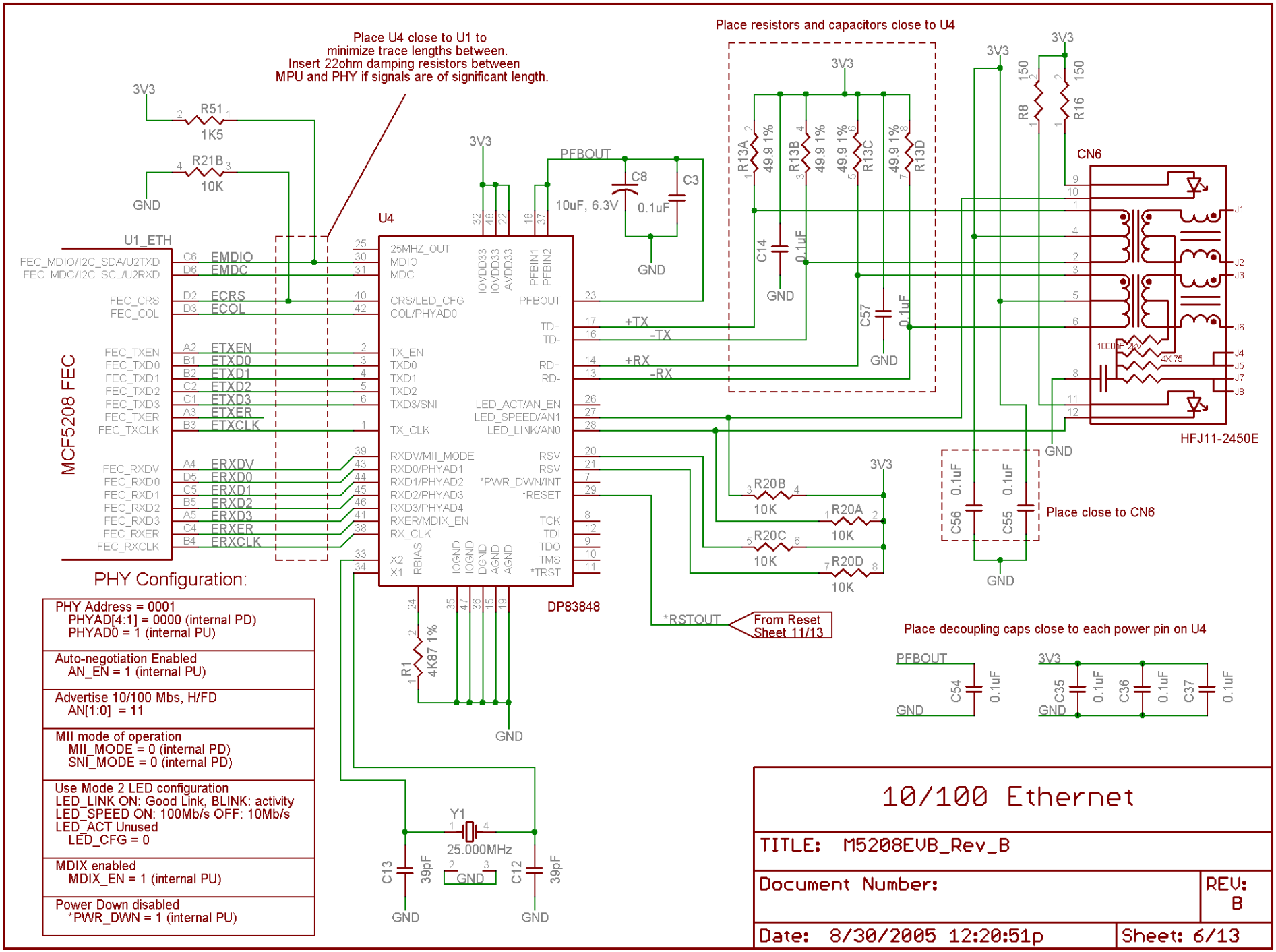

PHY Configuration:

PHY Address = 0001 PHYAD[4:1] = 0000 (internal PD) PHYAD0 = 1 (internal PU)
Auto-negotiation Enabled AN_EN = 1 (internal PU)
Advertise 10/100 Mbs, H/FD AN[1:0] = 11
MII mode of operation MII_MODE = 0 (internal PD) SNI_MODE = 0 (internal PD)
Use Mode 2 LED configuration LED_LINK ON: Good Link, BLINK: activity LED_SPEED ON: 100Mb/s OFF: 10Mb/s LED_ACT Unused LED_CFG = 0
MDIX enabled MDIX_EN = 1 (internal PU)
Power Down disabled *PWR_DWN = 1 (internal PU)

10/100 Ethernet

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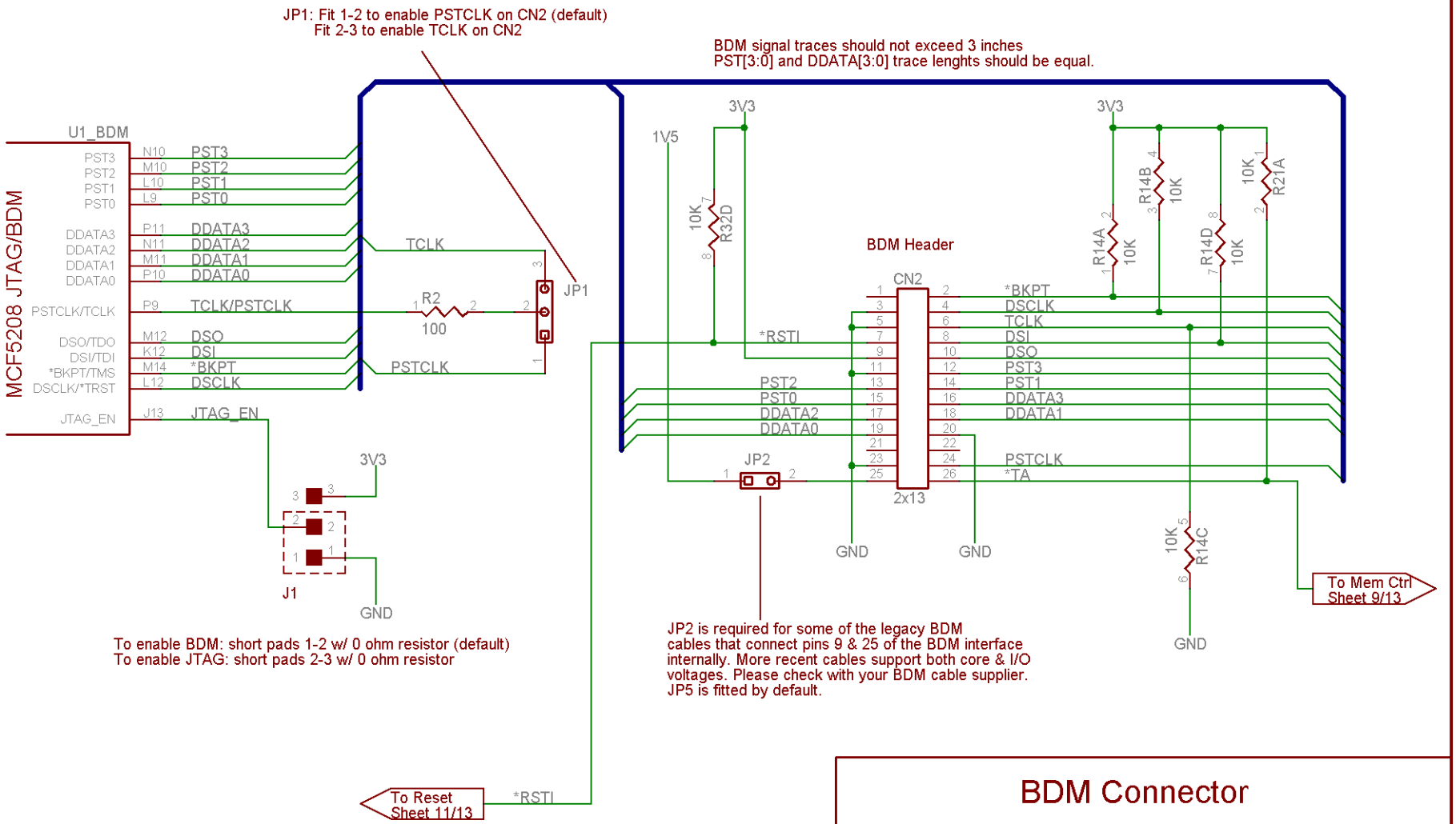

BDM Connector

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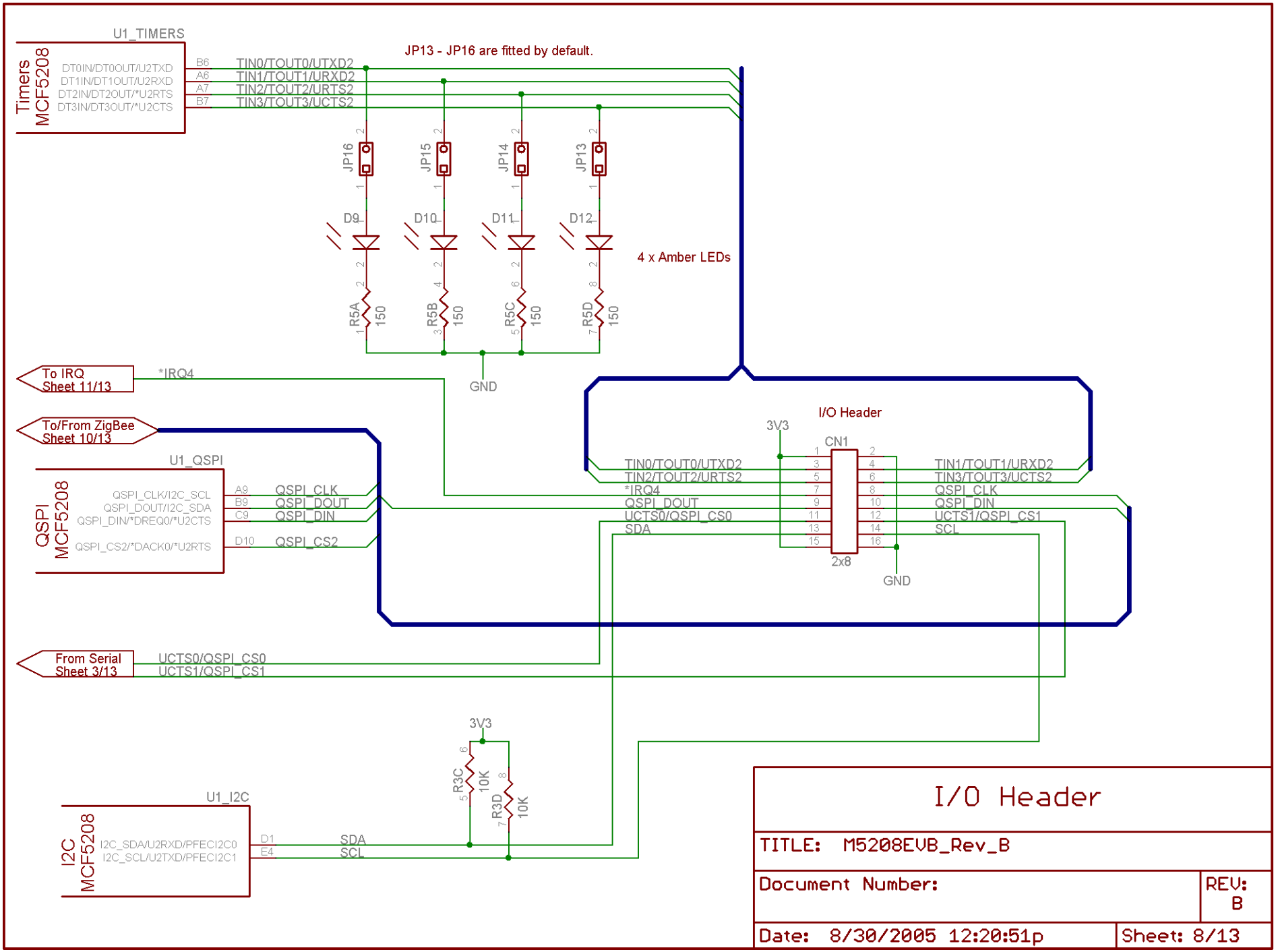
U1_TIMERS
Timers MCF5208
DT0IN/DT0OUT/U2TXD
DT1IN/DT1OUT/U2RXD
DT2IN/DT2OUT/*U2RTS
DT3IN/DT3OUT/*U2CTS
B6 TIN0/TOUT0/UTXD2
A6 TIN1/TOUT1/URXD2
A7 TIN2/TOUT2/URTS2
B7 TIN3/TOUT3/UCTS2
JP13 - JP16 are fitted by default.
JP16
JP15
JP14
JP13
D9
D10
D11
D12
4 x Amber LEDs
R5A 150
R5B 150
R5C 150
R5D 150
GND
To IRQ Sheet 11/13
*IRQ4
To/From ZigBee Sheet 10/13
I/O Header
3V3
CN1
TIN0/TOUT0/UTXD2
TIN2/TOUT2/URTS2
*IRQ4
QSPI_DOUT
UCTS0/QSPI_CS0
SDA
TIN1/TOUT1/URXD2
TIN3/TOUT3/UCTS2
QSPI_CLK
QSPI_DIN
UCTS1/QSPI_CS1
SCL
2x8
GND
U1_QSPI
QSPI MCF5208
QSPI_CLK/I2C_SCL
QSPI_DOUT/I2C_SDA
QSPI_DIN/*DREQ0/*U2CTS
QSPI_CS2/*DACK0/*U2RTS
A9 QSPI_CLK
B9 QSPI_DOUT
C9 QSPI_DIN
D10 QSPI_CS2
From Serial Sheet 3/13
UCTS0/QSPI_CS0
UCTS1/QSPI_CS1
3V3
R3C 10K
R3D 10K
U1_I2C
I2C MCF5208
I2C_SDA/U2RXD/PFECI2C0
I2C_SCL/U2TXD/PFECI2C1
D1 SDA
E4 SCL
I/O Header
TITLE: M5208EVB_Rev_B
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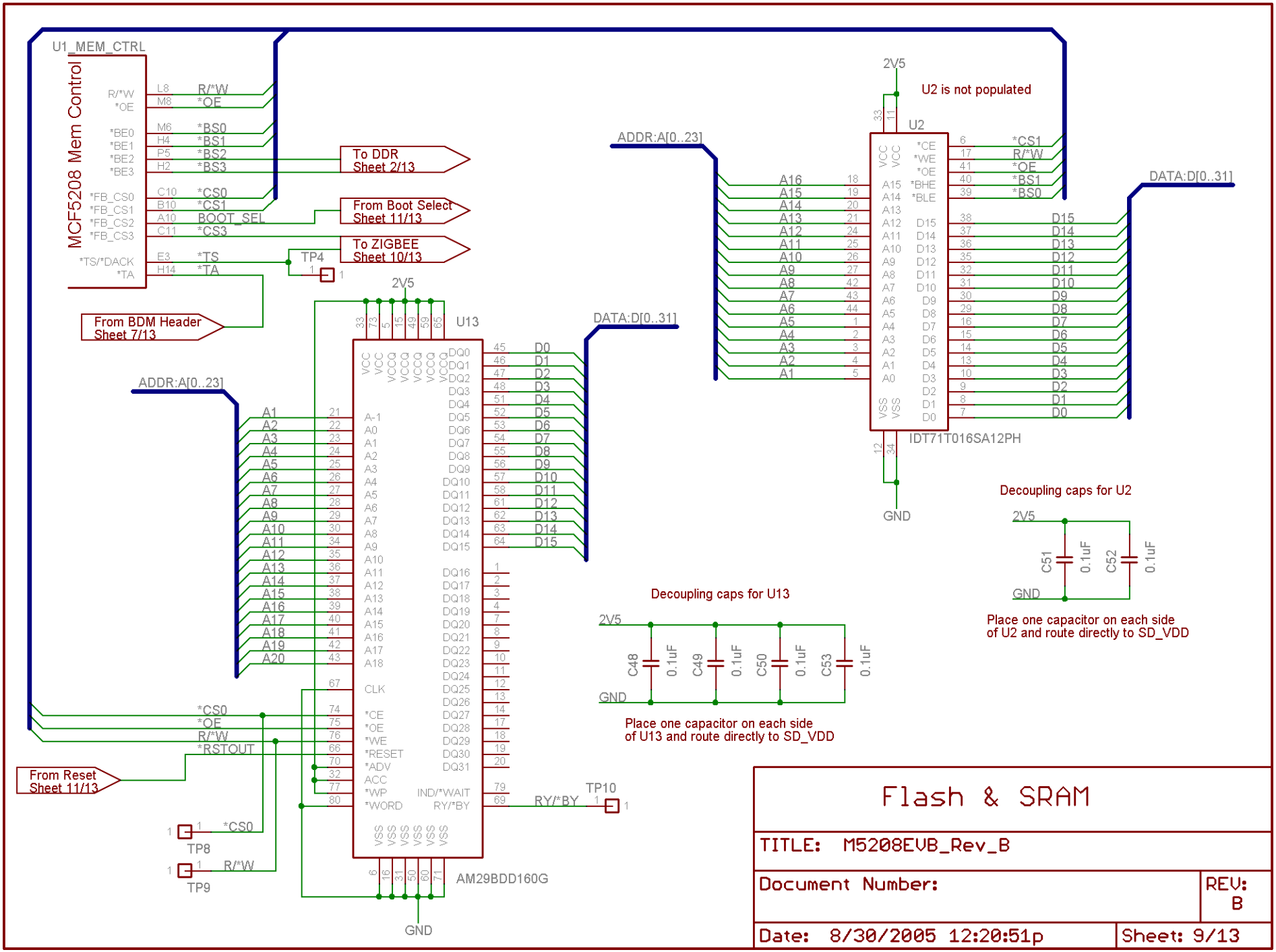
U1_MEM_CTRL
MCF5208 Mem Control
R/*W
*OE
*BE0
*BE1
*BE2
*BE3
*FB_CS0
*FB_CS1
*FB_CS2
*FB_CS3
*TS/*DACK
*TA
L8 R/*W
M8 *OE
M6 *BS0
H4 *BS1
P5 *BS2
H2 *BS3
C10 *CS0
B10 *CS1
A10 BOOT_SEL
C11 *CS3
E3 *TS
H14 *TA
To DDR Sheet 2/13
From Boot Select Sheet 11/13
To ZIGBEE Sheet 10/13
TP4
From BDM Header Sheet 7/13
2V5
U13
DATA:D[0..31]
ADDR:A[0..23]
AM29BDD160G
*CS0
*OE
R/*W
*RSTOUT
From Reset Sheet 11/13
TP8
TP9
TP10
RY/*BY
GND
U2 is not populated
U2
IDT71T016SA12PH
Decoupling caps for U13
C48 0.1uF
C49 0.1uF
C50 0.1uF
C53 0.1uF
Place one capacitor on each side of U13 and route directly to SD_VDD
Decoupling caps for U2
C51 0.1uF
C52 0.1uF
Place one capacitor on each side of U2 and route directly to SD_VDD
Flash & SRAM
TITLE: M5208EVB_Rev_B
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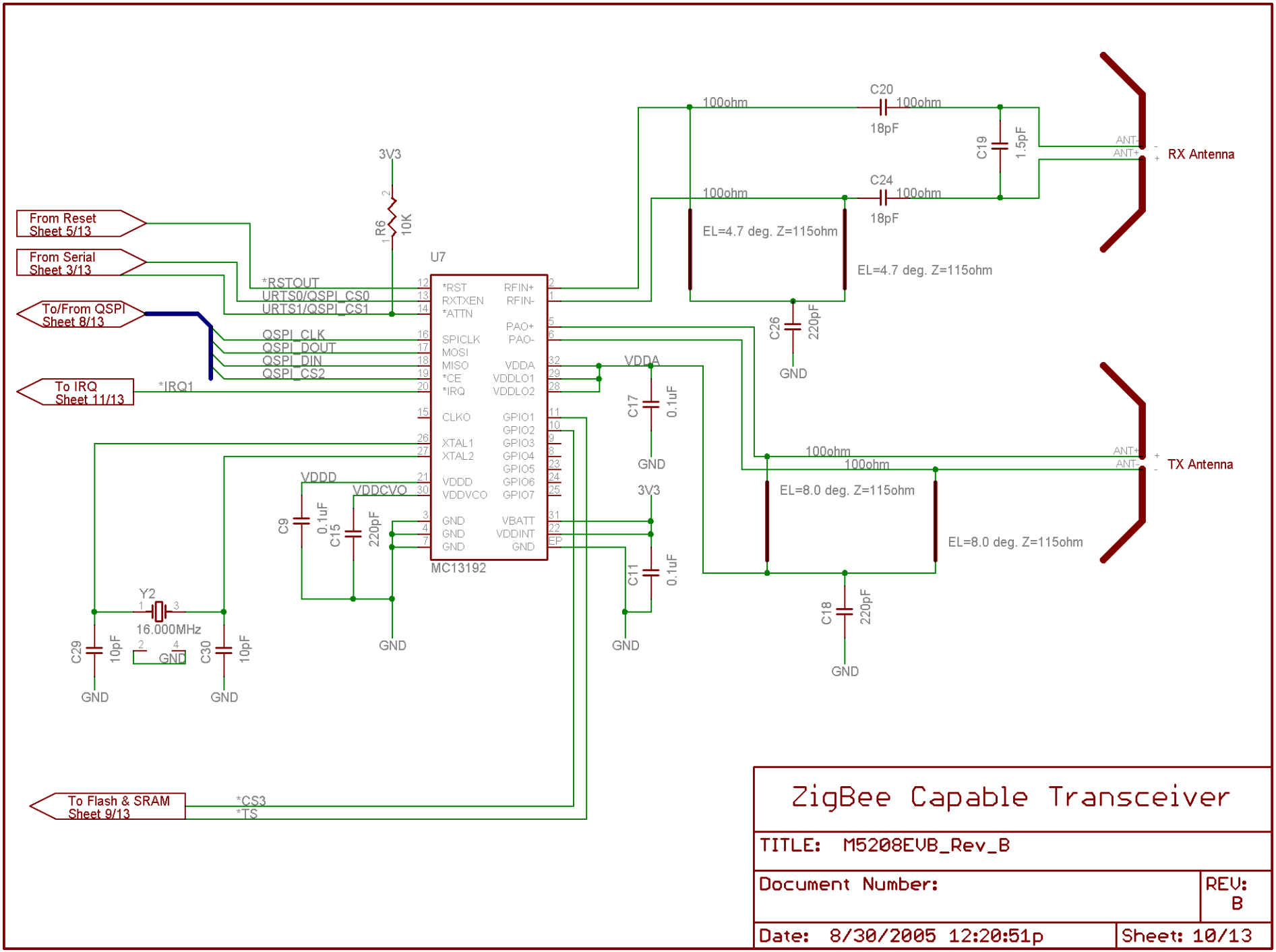

ZigBee Capable Transceiver

TITLE: M5208EVB_Rev_B	
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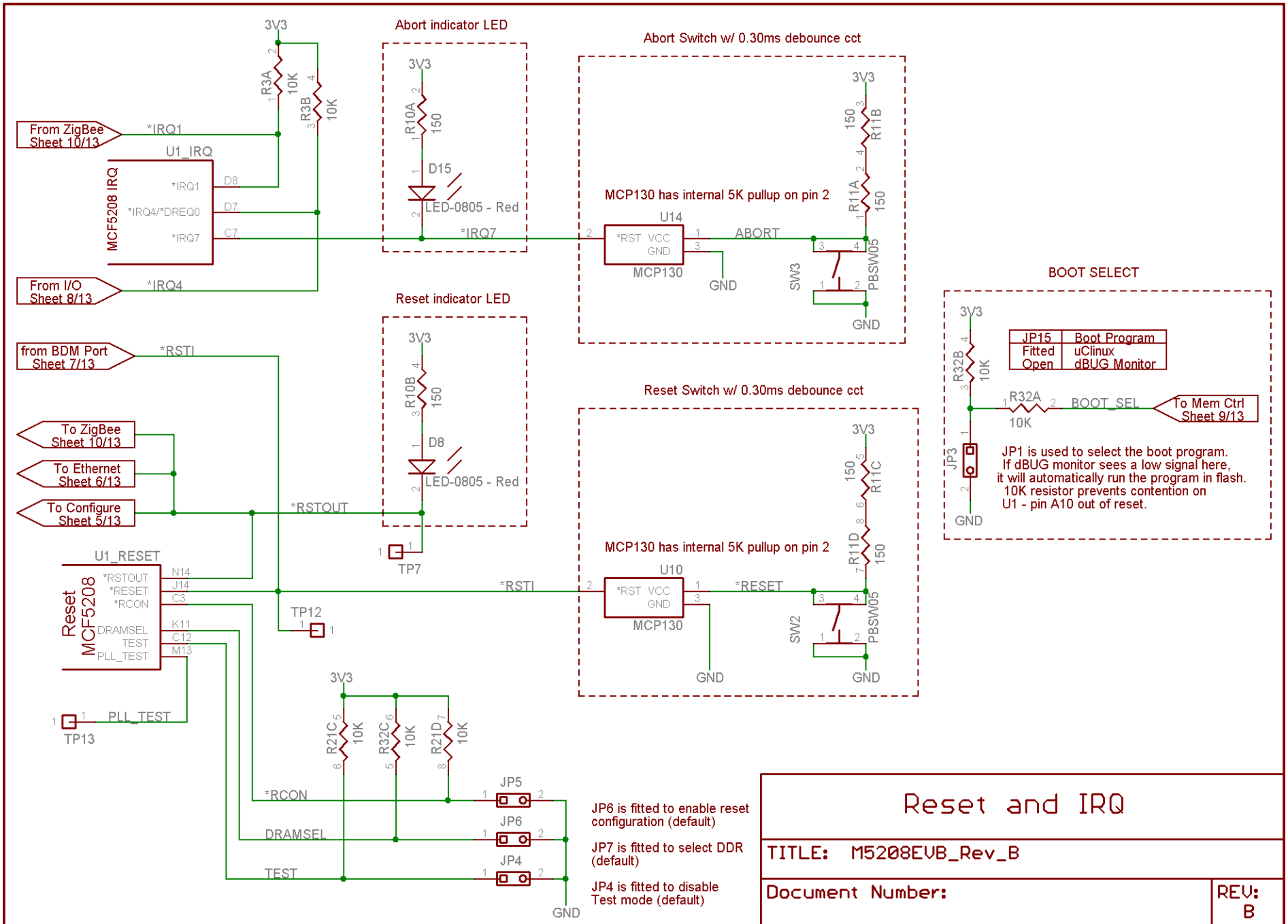
3V3
R3A
10K
R3B
10K
From ZigBee
Sheet 10/13
*IRQ1
U1_IRQ
MCF5208 IRQ
*IRQ1
*IRQ4/*DREQ0
*IRQ7
D8
D7
C7
From I/O
Sheet 8/13
*IRQ4
Abort indicator LED
R10A
150
D15
LED-0805 - Red
*IRQ7
Abort Switch w/ 0.30ms debounce cct
MCP130 has internal 5K pullup on pin 2
U14
*RST VCC
GND
MCP130
ABORT
GND
R11B
150
R11A
150
SW3
PBSW05
GND
BOOT SELECT
R32B
10K
JP15 Boot Program
Fitted uClinux
Open dBUG Monitor
R32A
10K
BOOT_SEL
To Mem Ctrl
Sheet 9/13
JP3
JP1 is used to select the boot program.
If dBUG monitor sees a low signal here,
it will automatically run the program in flash.
10K resistor prevents contention on
U1 - pin A10 out of reset.
GND
from BDM Port
Sheet 7/13
*RSTI
Reset indicator LED
R10B
150
D8
LED-0805 - Red
TP7
To ZigBee
Sheet 10/13
To Ethernet
Sheet 6/13
To Configure
Sheet 5/13
*RSTOUT
Reset Switch w/ 0.30ms debounce cct
MCP130 has internal 5K pullup on pin 2
U10
*RST VCC
GND
MCP130
*RESET
GND
R11C
150
R11D
150
SW2
PBSW05
GND
U1_RESET
Reset
MCF5208
*RSTOUT
*RESET
*RCON
DRAMSEL
TEST
PLL_TEST
N14
J14
C3
K11
C12
M13
TP12
TP13
PLL_TEST
R21C
10K
R32C
10K
R21D
10K
*RCON
DRAMSEL
TEST
JP5
JP6
JP4
GND
JP6 is fitted to enable reset configuration (default)
JP7 is fitted to select DDR (default)
JP4 is fitted to disable Test mode (default)
Reset and IRQ
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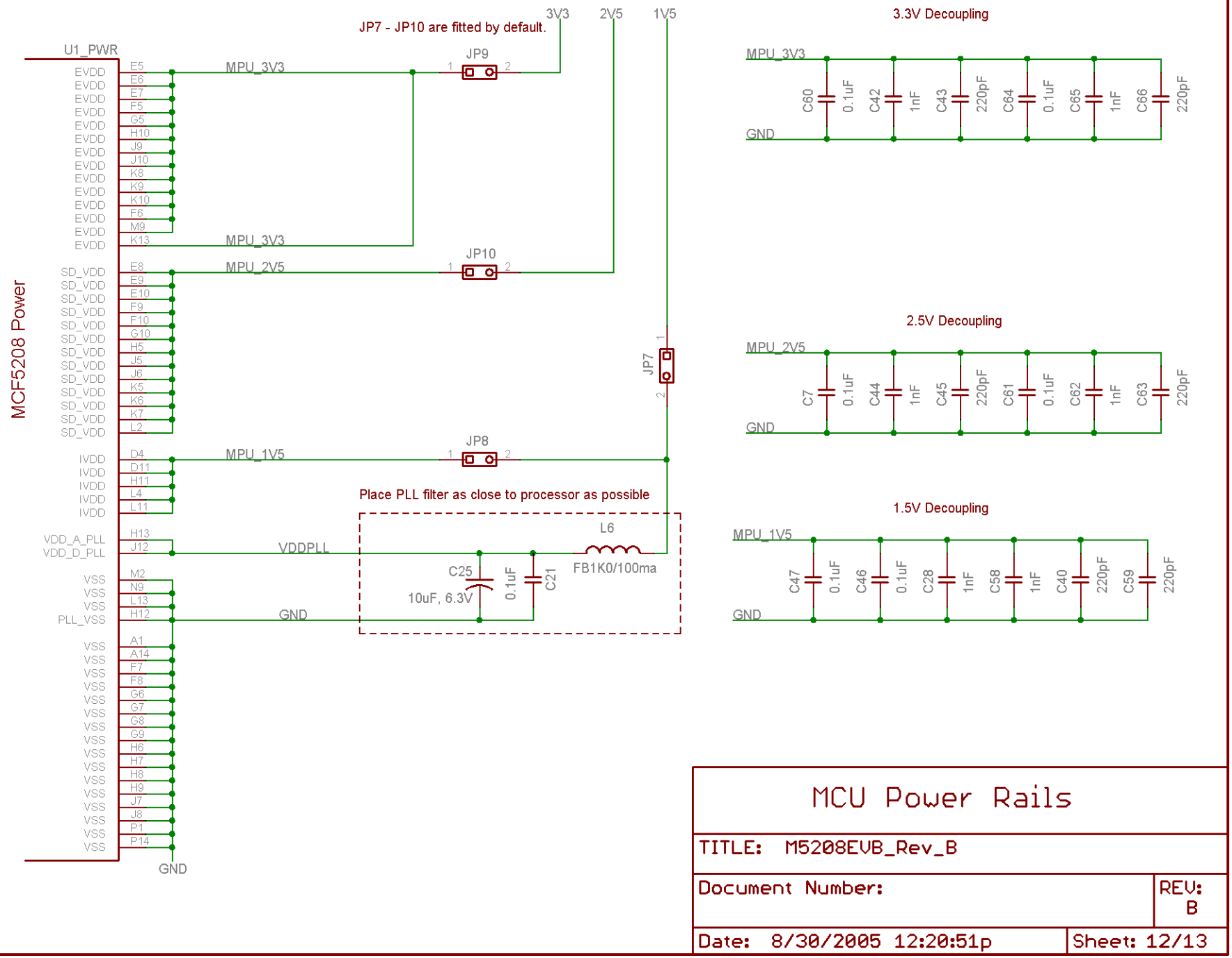

MCU Power Rails

TITLE: M5208EVB_Rev_B	
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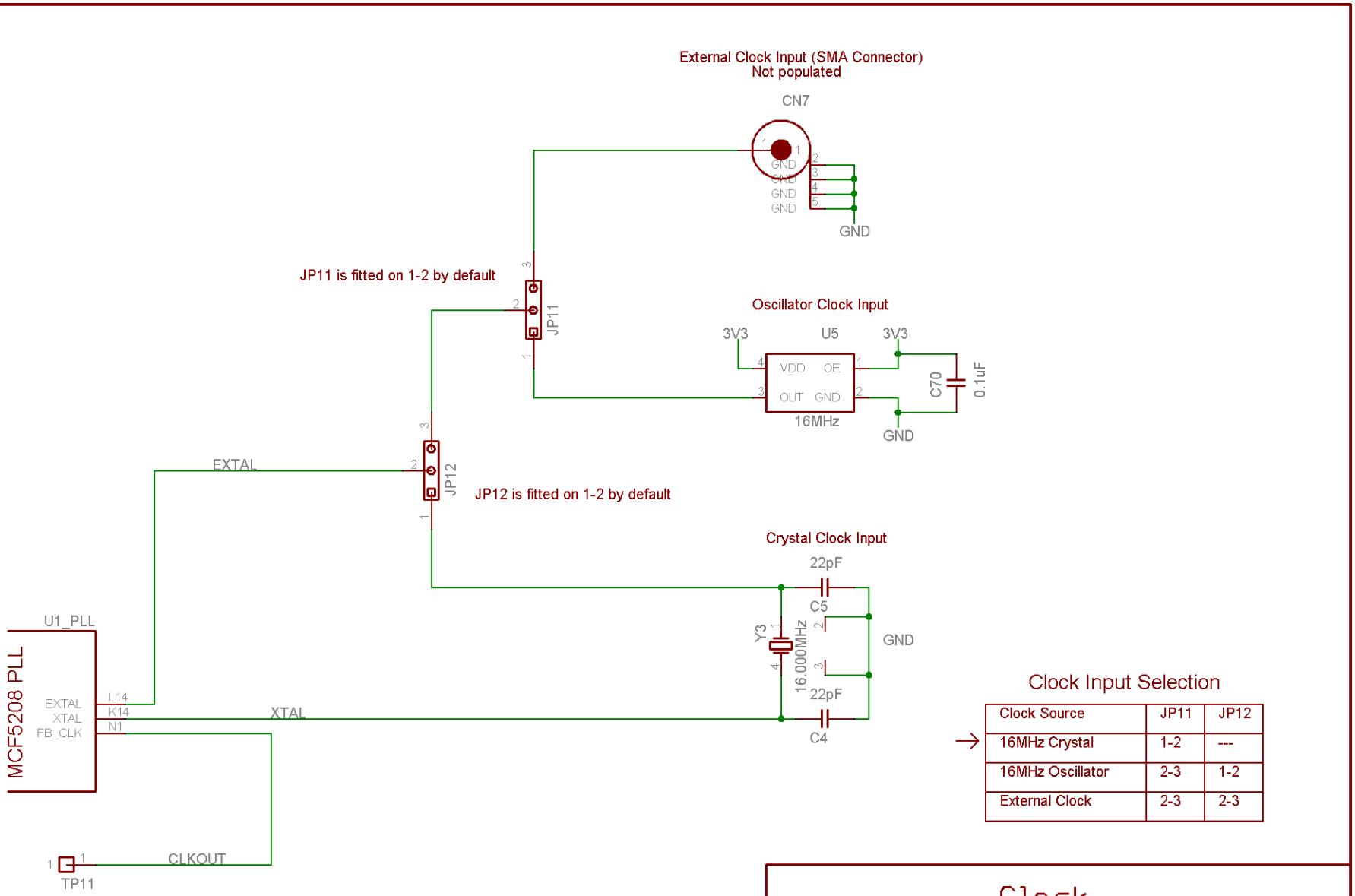
External Clock Input (SMA Connector)
Not populated
CN7
GND
GND
GND
GND
JP11 is fitted on 1-2 by default
JP11
Oscillator Clock Input
3V3
U5
3V3
VDD
OE
OUT
GND
16MHz
C70
0.1uF
GND
EXTAL
JP12
JP12 is fitted on 1-2 by default
Crystal Clock Input
22pF
C5
Y3
16.000MHz
GND
22pF
C4
U1_PLL
MCF5208 PLL
EXTAL
XTAL
FB_CLK
L14
K14
N1
XTAL
CLKOUT
TP11
Clock Input Selection
Clock Source | JP11 | JP12
16MHz Crystal | 1-2 | ---
16MHz Oscillator | 2-3 | 1-2
External Clock | 2-3 | 2-3
Clock
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